IN THE CLAIMS

Please amend the claims as follows:

1. (Six Times Amended) A semiconductor device comprising:

a first semiconductor layer having a first doping state of a first conductivity type and having first and second major surfaces;

a first semiconductor region of a second conductivity type formed selectively in said first major surface of said first semiconductor layer so that said first semiconductor layer [is exposed in] remains in the first doping state along a peripheral portion of said first major surface, and said first semiconductor layer [is exposed in] remains in the first doping state in [the] a form of an insular region in a planar view in a central portion of said first major surface;

a second semiconductor region of the first conductivity type formed in a surface of said first semiconductor region, with a channel region provided between said second semiconductor region and said insular region of said first semiconductor layer;

a gate insulating film formed on a surface of said channel region;

a first gate electrode from a plurality of gate electrodes formed on said gate insulating film;

an interlayer insulating film formed at least on said first gate electrode:

a first main electrode formed over a surface of said interlayer insulating film and covering a surface of said second semiconductor region, said first main electrode being electrically connected to said second semiconductor region and having an end extending to a boundary between the peripheral portion of said first major surface and the central portion of said first major surface;

a second main electrode formed on said second major surface of said first semiconductor layer; and

an integral semi-insulating plasma CVD nitride film covering at least the peripheral portion of said first major surface other than the central portion of said first major surface and not extending [to] above any gate electrode [an upper portion of said first gate], said integral semi-insulating plasma CVD nitride film having a conductivity which does not lose function as an insulating film and stabilizes breakdown voltage characteristics of the semiconductor device.

2. The semiconductor device of claim 1, wherein

said plasma CVD nitride film extends from the peripheral portion of said first major surface to a surface of said first main electrode at said end.

3. (Four Times Amended) The semiconductor device of claim 1, further comprising:

a second gate electrode from the plurality of gate electrodes not covered with said first main electrode [gate]; and

a gate interconnection line formed selectively on a surface of said second gate electrode,

wherein a trench is formed between said first main electrode and said gate interconnection line for electrical isolation between said first main electrode and said gate interconnect line, and

wherein said first gate electrode and said second gate electrode are integrally formed and electrically connected [by said gate interconnection line] to each other.

4. The semiconductor device of claim 3, wherein

said plasma CVD nitride film further extends from a surface of said gate interconnection line through said trench to a portion of a surface of said first main electrode.

5. The semiconductor device of claim 4, wherein

said plasma CVD nitride film is a semi-insulation film having a conductivity ranging from 1×10^{-14} to 1×10^{-10} ($1/\Omega$cm).

6. The semiconductor device of claim 4, wherein

said plasma CVD nitride film is a semi-insulation film having a conductivity ranging from 1×10^{-13} to 1×10^{-11} ($1/\Omega$cm).

7. The semiconductor device of claim 1, further comprising:

a second semiconductor layer of the second conductivity type formed between said second major surface of said first semiconductor layer and said second main electrode.

8. (Three Times Amended) The semiconductor device of claim 7, further comprising:

a second gate <u>electrode from the plurality of gate electrodes</u> not covered with said first main electrode; <u>and</u>

<u>a gate interconnection line formed selectively on a surface of said second gate electrode,</u>

wherein a trench is formed between said first main electrode and said gate interconnection line for electrical isolation between said first main electrode and said gate interconnect line, and

wherein said first gate electrode and said second gate electrode are integrally formed and electrically connected [by said gate interconnection line] to each other.

9. (Amended) The semiconductor device of claim 8, wherein

said [surface protective film] plasma CVD nitride film further extends from a surface of said gate interconnection line through said trench to a portion of a surface of said first main electrode.

10. The semiconductor device of claim 9, wherein

said plasma CVD nitride film is a semi-insulation film having a conductivity ranging from 1×10^{-14} to 1×10^{-10} ($1/\Omega$cm).

11. The semiconductor device of claim 9, wherein

said plasma CVD nitride film is a semi-insulation film having a conductivity ranging from 1×10^{-13} to 1×10^{-11} ($1/\Omega$cm).

12. (Seven Times Amended) A semiconductor device comprising:

a first semiconductor layer having a first doping state of a first conductivity type and having first and second major surfaces;

at least one first semiconductor region of a second conductivity type formed selectively in said first major surface of said first semiconductor layer so that said first semiconductor [layer is exposed in] remains in the first doping state along a peripheral portion of said first major surface, and said first semiconductor [layer is exposed in] region remains in the first doping state in [the] a form of a plurality of insular regions in a planar view in a central portion of said first major surface;

a plurality of second semiconductor regions of the first conductivity type formed in a surface of said at least one first semiconductor region, with channel regions provided between said second semiconductor regions and said insular regions of said first semiconductor layer;

a gate insulating film formed on a surface of said channel regions;

a first gate electrode from a plurality of gate electrodes formed on said gate insulating film;

an interlayer insulating film formed at least on said first gate electrode;

a first main electrode formed over a surface of said interlayer insulating film and covering a surface of said second semiconductor region, said first main electrode being electrically connected to said plurality of second semiconductor regions, said first main electrode further having an end extending to a boundary between the peripheral portion of said first major surface and the central portion of said first major surface;

a second main electrode formed on said second major surface of said first semiconductor layer; and

an integral semi-insulating plasma CVD nitride film for covering at least the peripheral portion of said first major surface other than the central portion of said first major surface and not extending [to] above any gate electrode [an upper portion of said first gate], said at least every first gate is formed, said integral semi-insulating plasma CVD nitride film having a conductivity which does not lose function as an insulating film and stabilizes breakdown voltage characteristics of the semiconductor device.

13. The semiconductor device of claim 12, wherein

said plasma CVD nitride film extends from the peripheral portion of said first major surface to a surface of said first main electrode at said end.

14. (Three Times Amended) The semiconductor device of claim 13, further comprising:

a second gate electrode from the plurality of gate electrodes not covered with said first main electrode; and

a gate interconnection line formed selectively on a surface of said second gate electrode,

wherein a trench is formed between said first main electrode and said gate interconnection line for electrical isolation between said first main electrode and said gate interconnect line, and

wherein said first gate electrode and said second gate electrode are integrally formed and electrically connected [by said gate interconnection line] to each other.

15. The semiconductor device of claim 14, wherein

said plasma CVD nitride film further extends from a surface of said gate interconnection line through said trench to a portion of a surface of said first main electrode.

16. The semiconductor device of claim 15, wherein

said plasma CVD nitride film is a semi-insulation film having a conductivity ranging from 1×10^{-14} to 1×10^{-10} ($1/\Omega$cm).

17. The semiconductor device of claim 15, wherein

said plasma CVD nitride film is a semi-insulation film having a conductivity ranging from 1×10^{-13} to 1×10^{-11} ($1/\Omega$cm).

18. The semiconductor device of claim 13, further comprising:

a second semiconductor layer of the second conductivity type formed between said second major surface of said first semiconductor layer and said second main electrode.

19. (Three Times Amended) The semiconductor device of claim 18, further comprising:

a second gate electrode from the plurality of gate electrodes not covered with said first main electrode; and

a gate interconnection line formed selectively on a surface of said second gate electrode,

wherein a trench is formed between said first main electrode and said gate interconnection line for electrical isolation between said first main electrode and said gate interconnect line, and

wherein said first gate electrode and said second gate electrode are integrally formed and electrically connected [by said gate interconnction line] to each other.

20. The semiconductor device of claim 19, wherein

said plasma CVD nitride film further extends from a surface of said gate interconnection line through said trench to a portion of a surface of said first main electrode.

21. The semiconductor device of claim 20, wherein

said plasma CVD nitride film is a semi-insulation film having a conductivity ranging from 1×10^{-14} to 1×10^{-10} ($1/\Omega$cm).

22. The semiconductor device of claim 20, wherein

said plasma CVD nitride film is a semi-insulation film having a conductivity ranging from 1×10^{-13} to 1×10^{-11} ($1/\Omega$cm).